CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values;

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer.

2. The computer system of Claim 1, wherein the rasterization circuit performs scan conversion on vertices having floating point color values.

3. The computer system of Claim 1 further comprising:

a texture circuit coupled to the rasterization circuit that applies a texture to the primitive, wherein the texture is specified by floating point values;

a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values.

4. The computer system of Claim 1, wherein the color values in the frame buffer are floating point color values.

5. The computer system of Claim 1, wherein the floating point format is comprised of sixteen bits.

6. The computer system of Claim 5, wherein the floating point format is comprised of an s10e5 format.

7. The computer system of Claim 1 further comprising a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on floating point color values.

8. The computer system of Claim 1 further comprising a fog circuit coupled to the rasterization circuit for performing a fog function, wherein the fog function operates on floating point color values.

9. The computer system of Claim 1 further comprising an antialiasing circuit coupled to the rasterization circuit which performs an antialiasing algorithm according to floating point color values.

10. The computer system of Claim 1 further comprising a blender coupled to the rasterization circuit which blends floating point color values.

11. The computer system of Claim 1 further comprising logic coupled to the rasterization circuit which performs per-fragment operations on floating point color values.

12. The computer system of Claim 1, wherein the processor, the rasterization circuit, and the frame buffer are on a single semiconductor chip.

13. The computer system of Claim 12, wherein the processor, the rasterization circuit, and the frame buffer reside on a same substrate of the single semiconductor chip.

14. In a computer system, a method for rendering a three-dimensional image for display, comprising the steps of:

performing geometric calculations on a plurality of vertices of a plurality of polygons;

scan converting a plurality of pixels according to the vertices, wherein scan conversion is performed on floating point color values;

applying a texture to the image by reading floating point texture values stored in a texture memory;

simulating fog effects, wherein fog is simulated by modifying floating point color values;

drawing the image for display on a display screen coupled to the computer system.

15. The method of Claim 13, wherein the floating point values are comprised of sixteen bits.

16. The method of Claim 15, wherein the floating point values are specified by a s10e5 format.

17. The method of Claim 15 further comprising the step of storing the floating point color values in a frame buffer.

18. The method of Claim 15 further comprising the step of blending at least two floating point color values.

19. The method of Claim 15 further comprising the step of performing antialiasing on floating point color values.

20. The method of Claim 15 further comprising the steps of:

reading data from the frame buffer;

modifying the data;

writing modified data back to the frame buffer.

21. The method of Claim 15 further comprising the step of modifying color values for lighting, wherein lighting calculations operate on floating point color values.

22. In a computer system, a method for operating on data stored in a frame buffer, comprised of:

storing the data in the frame buffer in a floating point format;

reading the data from the frame buffer in the floating point format;

operating directly on the data in the floating point format;

writing the data to the frame buffer in the floating point format.

23. The method of Claim 22, wherein the data are written to a frame buffer in a floating point format.

24. The method of Claim 22, wherein the data are read from the frame buffer in a floating point format.

25. The method of Claim 22, wherein the data are stored in a frame buffer in a floating point format.

26. The method of Claim 22, wherein the steps of writing, storing, and reading the data in the frame buffer in a floating point format is further comprised of a specification of the floating point format, wherein the

specification corresponds to a level of range and precision.

27. The method of Claim 26 wherein the specification is comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits.

28. The method of Claim 26 wherein the specification is comprised of 17 bits of data and the data are comprised of one sign bit, 11 mantissa bits, and five exponent bits.

29. The method of Claim 26 wherein the specification is comprised of 16 bits of data and the data are comprised of ten mantissa bits, and six exponent bits.

30. The method of Claim 26 wherein the specification is comprised of 32 bits of data and the data are comprised of one sign bit, 23 mantissa bits, and eight exponent bits.

31. A computer system having a floating point frame buffer for storing a plurality of floating point color values.

32. The computer system of Claim 31, wherein the floating point color values are written to a frame buffer.

33. The computer system of Claim 31, wherein the floating point color values are read from a frame buffer.

34. The computer system of Claim 31, wherein the floating point color values are stored in a frame buffer.

35. The computer system of Claim 31, wherein the floating point color values are written to, read from, and stored in a frame buffer using a specification of the floating point values that corresponds to a level of range and precision.

36. The computer system of Claim 35, wherein the floating point color values are comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits.

37. The computer system of Claim 35, wherein the floating point color values are comprised of 17 bits of data and the data are comprised of one sign bit, 11 mantissa bits, and five exponent bits.

38. A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on an s10e5 floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of s10e5 floating point color values;

a display screen coupled to the frame buffer for displaying an image according to the s10e5 color values stored in the frame buffer.

39. The computer system of Claim 38 further comprising:

a texture circuit coupled to the rasterization circuit that applies a texture to the primitive, wherein the texture is specified by s10e5 floating point values.

40. The computer system of Claim 38 further comprising a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on s10e5 floating point color values.

41. The computer system of Claim 38 further comprising a fog circuit coupled to the rasterization circuit for performing a fog function, wherein the fog function operates on s10e5 floating point color values.

42. The computer system of Claim 38 further comprising an antialiasing circuit coupled to the rasterization circuit which performs an antialiasing algorithm on s10e5 floating point color values.

43. The computer system of Claim 38 further comprising a blender coupled to the rasterization circuit which blends s10e5 floating point color values.

44. The computer system of Claim 38 further comprising logic coupled to the rasterization circuit which performs per-fragment operations on s10e5 floating point color values.